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EXAMINER	
PAREKH, NITIN	
ART UNIT	**PAPER NUMBER**
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/652,495	AKRAM, SALMAN	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-41 and 43-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-41 and 43-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08-31-2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 5-10, 15, 18, 19, 21, 22, 26-28, 30-36, 43, 44 and 50-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 6004867) in view of Lin (US Pat. 5258648).

Regarding claim 1, Kim et al. disclose a chip scale package (CSP)/flip chip carrier (FCC) comprising:

- a semiconductor device/silicon chip (110 in Fig. 2) including an active surface having bond pads (112 in Fig. 2), the device being invertedly disposed on a first surface of a substrate (120 in Fig. 2)
- the substrate comprising a semiconductor material such as silicon (Col. 3, line 51) having substantially the same coefficient of thermal expansion (CTE) as that of the device/chip, the substrate having conductive traces (122 in Fig. 2) on a first surface, being disposed adjacent the active surface of the device and the

substrate including a plurality of electrically conductive vias extending partially there-through, the vias filled with an electrically conductive material (123 in Fig. 2; Col. 4, line 15), the vias having one end being in communication with/bonded to the conductive traces/contact areas and corresponding bond pads (122 and 112 respectively in Fig. 2) of the device

- an intermediate/passivation layer (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate, and
- electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from a second surface, the second surface being opposite to the first surface and the bumps being in communication with respective electrically conductive vias

(Fig. 1 and 2; Col. 2, line 62- Col. 4, line 40).

Kim et al. further disclose:

- forming direct vertical/via connections between vertically separated trace/metal layers using through-holes extending through the substrate (not numerically referenced in Fig. 1-3; Col. 4, line 55) providing an alignment of the vias and respective bond pads, and
- forming traces (122 in Fig. 2) anywhere in the substrate (top/bottom, middle layer, etc.-see Fig. 2 and 3; Col. 3, line 55) and forming the vias and pads (124/123 in Fig. 2) at any desired position on the surface of the substrate with respect to the position of the chip pads (Col. 4, line 9-25).

Kim et al. fail to teach at least one conductive trace in communication with at least one electrically conductive via, the trace being carried on the second surface.

Lin teaches using a semiconductor device package (Fig. 4) comprising a substrate/interposer (22 in Fig. 3-6) having a surface adjacent to a device/chip (12 in Fig. 3-6) and an opposite surface, the substrate having electrically conductive vias (24 in Fig. 3 and 4) extending there-through (Col. 5, line 1-5) and solder balls/bumps (32 in Fig. 3, 4 and 6) connected at the ends of the vias. Lin further teaches the substrate having conductive traces in communication of the vias/solder balls at both ends, the traces being carried on the opposite surface/bottom surface in lateral directions from the vias (see traces 43/44 with respect to the solder balls/vias in Fig. 6; Col. 8, line 55-60; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least one conductive trace in communication with at least one electrically conductive via, the trace being carried on the second surface of the substrate as taught by Lin so that the desired routing for the vias and power/ground connections for the terminals/solder balls can be achieved in Kim et al's package.

Regarding claim 2, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. further teach:

- electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from the second surface and the bumps being in communication with the electrically conductive vias (Fig. 1 and 2; Col. 2, line 62-Col. 4, line 40), and

- the vias being formed by plated layers/traces of one or more barrier metals (Col. 4, lines 13-16; Col. 3, lines 63-65) such that the solder bumps are located on another end/opposite end of the plated layer/trace from the respective via.

Regarding claim 3, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the electrically conductive vias extending substantially/directly through the substrate.

Regarding claim 5, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the substrate of the semiconductor device and the substrate comprising the same type of semiconductor material such as silicon.

Regarding claim 6, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the substrate of the device and the substrate comprising the semiconductor materials having substantially the same CTE.

Regarding claim 7, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the substrate of the device comprising silicon.

Regarding claim 8, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the semiconductor material comprising silicon.

Regarding claim 9, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, and Kim et al. further teach a first thickness of the semiconductor device/chip (110 in Fig. 2) being greater than that of the semiconductor substrate (120 in Fig. 2), but fail to specify those being substantially the same.

Lin teaches using the chip and the substrate (12 and 22 respectively in Fig. 1 and 3) having respective first and second thicknesses being substantially the same.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device and the substrate having substantially the same thickness as taught by Lin so that manufacturing yield and cycle time can be improved in Kim et al's package.

Regarding claim 10, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, and Kim et al. further teach the first thickness of the semiconductor device/chip (110 in Fig. 2) being greater than that of the semiconductor substrate (120 in Fig. 2).

Regarding claims 15 and 18, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, and Kim et al. further teach the intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate adhering the device and the substrate and the conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 19, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the electrically conductive vias/conductive material being bonded/electrically connected to the corresponding bond pads.

Regarding claim 21, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, wherein Kim et al. teach the device being invertedly disposed adjacent the substrate.

Regarding claim 22, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 1 and 21 above, wherein Kim et al. teach the bond pads contacting the corresponding vias.

Regarding claim 26, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 15 above, wherein Kim et al. teach the intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate and the electrically conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 27, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 18 above, wherein Kim et al. teach the electrically conductive vias, conductive traces and corresponding bond pads being in communication through the intermediate layer.

Regarding claim 28, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 15 above, wherein Kim et al. teach using the intermediate/passivation layer adhering the device to the substrate.

Regarding claim 30, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 2 above, wherein Kim et al. further teach:

- electrically conductive metal bumps (130 in Fig. 2) such as solder (Col. 4, line 27; Col. 6, line 60) protruding from the second surface opposite to the one adjacent the device and the bumps being in communication with the electrically conductive vias (Fig. 1 and 2; Col. 2, line 62- Col. 4, line 40), and
- the vias being formed by plated layers/traces of one or more barrier metals (Col. 4, lines 13-16; Col. 3, lines 63-65) such that the solder bumps are located on another end/opposite end of the plated layer/trace from the respective via.

Regarding claim 31, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 2 above, wherein Kim et al. teach the conductive metal bumps being solder.

Regarding claim 32, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 1 above, wherein Kim et al. teach the semiconductor device and the substrate comprising the same type of semiconductor material.

Regarding claim 33, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 1 above, wherein Kim et al. teach the semiconductor device and the substrate comprising the same type of semiconductor material such as silicon.

Regarding claim 34, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 1 above, wherein Kim et al. teach the substrate of the semiconductor device comprising silicon.

Regarding claim 35, Kim et al. teach substantially the entire claimed structure as applied to claims 1 and 21 above, except the substrate and the device having substantially equal first and second thicknesses respectively.

As explained above for claim 9, Lin teaches using the chip and the substrate (12 and 22 respectively in Fig. 1 and 3) having respective first and second thicknesses being substantially the same.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the semiconductor device and the substrate having substantially the same thickness as taught by Lin so that manufacturing yield and cycle time can be improved in Kim et al's package.

Regarding claim 36, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 21 and 1 above, wherein Kim et al. teach the thickness of the semiconductor substrate being less than that of the semiconductor device/chip.

Regarding claim 43, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, including a CSP having a flip chip carrier (FCC) where a first end of the vias being positioned to substantially align with the corresponding bond pads of the chip and at least one conductive trace laterally extending from a second end of the via and being carried on the second/another surface which is opposite from the surface adjacent to the device.

Regarding claim 44, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, wherein Kim et al. teach the vias comprising the electrically conductive material.

Regarding claim 50, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, wherein Kim et al. teach the substrate comprising silicon.

Regarding claim 51, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, except using a conductive bump adjacent an end of at least one of the conductive traces located opposite to the second end of at least one via.

As explained above for claim 1, Lin teaches using a semiconductor device package (Fig. 4) comprising a substrate/interposer (22 in Fig. 3-6) having the first surface adjacent to a device/chip (12 in Fig. 3-6) and the second/bottom surface, the substrate having electrically conductive vias (24 in Fig. 3 and 4) extending there-through (Col. 5, line 1-5) and solder balls/bumps (32 in Fig. 3, 4 and 6) connected at the ends of the vias. Lin further teaches the substrate having conductive traces in communication of

the vias/solder balls at both ends, the traces being carried on the second surface/bottom surface (Col. 8, line 55-60; 42/44 in Fig. 6; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a conductive bump adjacent an end of at least one of the conductive traces located opposite to the second end of at least one via as taught by Lin so that the desired routing for the vias and power/ground connections for the terminals/solder balls can be achieved and the wiring resistance can be reduced in Kim et al's package.

Regarding claim 52, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, wherein Kim et al. teach the bumps comprising solder.

3. Claims 11-14, 20, 23-25, 37-41 and 45-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US Pat. 6004867) and Lin (US Pat. 5258648) as applied to claims 1, 21 and 43 above, and further in view of Gnadinger (US Pat. 5229647).

Regarding claim 11, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, but fail to specify the second surface of the substrate being partially coated with an insulating material.

Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the second surface of the substrate being partially coated with an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 12, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, but fail to specify an insulative material comprising a layer extending substantially over the second surface of the substrate.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over the second surface as taught by Gnadinger so that the

passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 13, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, but fail to specify an insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a wafer level packaging where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 14, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, but fail to specify an insulative material comprising a silicon oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that

having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising a silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 20, as explained above for claim 1, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 1 above, including a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad and via material.

Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Lin and Kim et al's package.

Regarding claim 23, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, including a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad via and respective material.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region comprising the bond pad and via as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Lin and Kim et al's package.

Regarding claim 24, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, including a region comprising bond pad, via and respective material but fail to specify forming a diffusion region comprising a bond pad and via material.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region comprising the bond pad and via material as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Lin and Kim et al's package.

Regarding claim 25, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, including a region comprising bond pad, via and respective material but fail to specify forming a diffusion region at least partially securing the device to the substrate.

As explained above for claim 20, Gnadinger teaches using a multichip package where a diffusion region is formed comprising via, bond pad and their material, the region securing the device to the substrate (23 in Fig. 4; Col. 4, line 23).

It would have been obvious to one of ordinary skill in the art at the time invention was made incorporate a diffusion region between the bond pad and via, the region securing the device to the substrate as taught by Gnadinger so that the metallurgical bonding and electrical performance of the device can be improved in Lin and Kim et al's package.

Regarding claim 37, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify at least a portion of the second surface of the substrate comprising an insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least a portion of the second surface of the substrate comprising an insulating material as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 38, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify at least one of the conductive vias being exposed through the insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the vias being exposed through the insulating material as taught by Gnadinger so that the bonding strength and interconnect reliability can be improved in Lin and Kim et al's package.

Regarding claim 39, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify an insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 40, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify an insulative material comprising silicon oxide.

As explained above for claim 11, Gnadinger teaches using a wafer level packaging where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 41, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify an insulative material comprising a layer extending substantially over the second surface of the substrate.

As explained above for claim 12, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over the second surface as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 45, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify an insulating material being disposed on at least a portion of at least one surface of the substrate.

Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material being disposed on at least a portion of at least one surface of the substrate as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 46, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify the insulative material comprising an oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising an oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 47, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify an insulative material comprising a silicon oxide.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the insulating material comprising a silicon oxide as taught by Gnadinger so that the passivation and surface protection for the substrate can be improved in Kim et al's package.

Regarding claim 48, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify an insulative material comprising a layer extending substantially over at least one surface of the substrate.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the substrate having the insulating material extending substantially over at least one surface as taught by Gnadinger so that the

passivation and surface protection for the substrate can be improved in Lin and Kim et al's package.

Regarding claim 49, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify the vias being exposed through the insulating material.

As explained above for claim 11, Gnadinger teaches using a multichip package where silicon/wafer substrates having aligned vias and bumps (21 and 28 respectively in Fig. 4) are formed with an insulating layer (24 in Fig. 4) such as a silicon oxide, nitride, etc., the insulating layer extending over the substrate surface opposite to that having device pads and the vias being exposed through the insulating material (Col. 4, line 28).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the vias being exposed through the insulating material as taught by Gnadinger so that the bonding strength and interconnect reliability can be improved in Lin and Kim et al's package.

4. Claims 16, 17, 29 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al (US Pat. 6004867) and Lin (US Pat. 5258648) as applied to claims 1, 21 and 43 above, and further in view of Higgins, III (US Pat. 6294405).

Regarding claim 16, Kim et al and Lin teach substantially the entire claimed structure as applied to claim 1 above, including an intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the

substrate but fail to specify using the intermediate layer comprising an adhesive material.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection and bonding/adhesion for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising an adhesive material as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claim 17, Kim et al. and Lin teach substantially the entire claimed structure as applied to claims 1 and 15 above, including an intermediate/passivation layer of silicon oxide or nitride (114 in Fig. 2; Col. 3, line-5) being disposed between the device and the substrate, but fail to specify using the intermediate layer comprising polyimide.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising polyimide as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claim 29, Kim et al and Lin teach substantially the entire claimed structure as applied to claim 21 above, but fail to specify using the intermediate layer comprising polyimide.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising polyimide as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claim 53, Kim et al and Lin teach substantially the entire claimed structure as applied to claims 1, 15 and 43 above, but fail to specify using an adhesive layer disposed adjacent the first surface of the substrate.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide/solder mask, silicon oxide, nitride, etc. (Col. 2, line 65, Col. 3, line 25-40) on a first surface of the chip/substrate to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an adhesive layer disposed adjacent the first surface of the substrate as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claim 54, Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify the adhesive layer comprising polyimide.

As explained above for claim 15 Higgins, III teaches, Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide/solder mask, silicon oxide, nitride, etc. (Col. 2, line 65, Col. 3, line 25-40) on a first surface of the chip/substrate to provide a protection for the device in a CSP. using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide, silicon oxide, nitride, etc. (Col. 2, line 65) to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an intermediate layer comprising polyimide as taught by Higgins, III so that the passivation and surface protection can be improved in Lin and Kim et al's package.

Regarding claim 55, Kim et al. and Lin Kim et al. and Lin teach substantially the entire claimed structure as applied to claim 43 above, but fail to specify the first ends of the vias extending through the adhesive layer.

Higgins, III teaches using an intermediate passivation/adhesion layer (18 in Fig. 1) such as polyimide/solder mask, silicon oxide, nitride, etc. (Col. 2, line 65, Col. 3, line 25-40) on a first surface of the chip/substrate to provide a protection for the device in a CSP.

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first ends of the vias extending through the

adhesive layer as taught by Higgins, III so that the bonding strength and interconnect reliability can be improved in Lin and Kim et al's package.

Response to Arguments

5. Applicant's arguments filed on 04-07-05 have been fully considered but they are not persuasive.

A. Applicant contends that Kim et al. and Lin, taken alone or together, lacks the interposer substrate including the second surface carrying at least one conductive trace, since Lin teaches the conductive traces on the surface of the interposer adjacent to the active surface of the die as shown in Fig. 1 and 5E.

However, as explained above, Lin clearly teaches the interposer substrate having electrical circuitry/conductive traces being in communication of the vias/solder balls at both surfaces of the interposer including the second/bottom surface as shown in Fig. 6 (Col. 7, lines 35-55). Such traces being not only on the top/first surface, which is adjacent and facing the device/chip, but are also carried on the bottom surface/second surface in different lateral directions perpendicular to the vias (see wiring/traces 44/43 connecting solder balls 42 in Fig. 6; Col. 8, line 55-60;) to provide the desired wiring/routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

B. Applicant contends that there is no motivation to combine Kim et al. and Lin to incorporate the conductive trace being carried on the second surface of the substrate

because such conductive traces on the second surface would increase the cost of manufacturing Kim et al's device.

However, as explained above, Lin teaches the electrical circuitry/conductive traces being carried on the second/bottom surface in lateral directions from the vias (see traces 43/44 with respect to the solder balls/vias in Fig. 6; Col. 8, line 55-60; Col. 7, line 35-55) to provide the desired routing for the vias and power/ground connections for the terminals/solder balls (Col. 6-8).

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAN or Public PAG. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAG system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

NP

06-16-05

NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800